Amendments to the Claims:

Please add new claims 21 and 22. Please amend claims 1, 8, 14, and 17 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A semiconductor memory device comprising:

a memory cell array including a plurality of memory cells connected between a plurality of word lines and a plurality of bit line pairs;

a predetermined number of write line pairs;

a predetermined number of read line pairs;

at least one data input pad;

at least one data output pad;

a data input circuit between the at least one data input pad and the predetermined number of write line pairs for transmitting first data which is applied through the at least one data input pad[[s]] to the predetermined number of write line pairs as second data during a write operation;

a plurality of write column selection gates for receiving the first data from the data input circuit and transmitting the second data between the plurality of bit line pairs and the predetermined number of write line pairs in response to a write column selection signal during the write operation;

a plurality of read column selection gates for transmitting third data between the plurality of bit line pairs and the predetermined number of read line pairs in response to a read column selection signal during a read operation; and

a data output circuit between the at least one data output pad and the predetermined number of read line pairs for outputting the third data as fourth data during the read operation, wherein the fourth data is output through the at least one data output pad[[s]], and wherein the first data is input through the at least one data input pad[[s]] during the write operation and the fourth data is output through the at least one data output pad[[s]] during the read operation simultaneously.

2. (Original) The semiconductor memory device according to claim 1, further comprising a command decoder for decoding externally input command signals and generating a write command for the write operation and a read command for the read operation.

3. (Previously Presented) The semiconductor memory device according to claim 2, wherein the command decoder further decodes the command signals to generate write and read commands for performing the write and read operations simultaneously.

4. (Previously Presented) A semiconductor memory device comprising:

a memory cell array including a plurality of memory cell array blocks each including a plurality of memory cells connected between a plurality of word lines and a plurality of bit line pairs;

a predetermined number of local write line pairs of each of the plurality of memory cell array blocks for inputting data in each of the plurality of memory cell array blocks;

a predetermined number of local read line pairs of each of the plurality of memory cell array blocks for outputting data of each of the plurality of memory cell array blocks;

a plurality of write column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local write line pairs during a write operation;

read column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local read line pairs during a read operation;

a predetermined number of global write line pairs connected to the predetermined number of local write line pairs of each of the plurality of memory cell array blocks;

a predetermined number of global read line pairs connected to the predetermined number of local read line pairs of each of the plurality of memory cell array blocks;

a first switch for transmitting data input through a predetermined number of data input pads to the predetermined number of global line pairs in response to a control signal, and outputting data transmitted from the predetermined number of global read line pairs to a

predetermined number of data output pads; and

a second switch for transmitting data input through the predetermined number of data output pads to the predetermined number of global line pairs in response to an inverted signal of the control signal, and outputting data transmitted from the predetermined number of global read line pairs to the predetermined number of data input pads.

5. (Original) The semiconductor memory device according to claim 4, further comprising a command decoder for decoding externaly input command signals and generating a write command for the write operation and a read command for the read operation.

6. (Previously Presented) The semiconductor memory device according to claim 5, wherein the command decoder further generates write and read commands for performing the write and the read operations simultaneously after decoding the commands.

7. (Canceled)

8. (Currently Amended) A semiconductor memory device comprising:

a memory cell array including a plurality of memory cell array blocks each including a plurality of memory cells connected between a plurality of word lines and a plurality of bit line pairs;

a predetermined number of local write line pairs of each of the plurality of memory cell array blocks for inputting data in each of the plurality of memory cell array blocks;

a predetermined number of local read line pairs of each of the plurality of memory cell array blocks for outputting data of each of the plurality of memory cell array blocks;

at least one data input pad;

at least one data output pad;

a plurality of write column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local write line pairs in response to write column selection signals during a write operation;

read column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local read line pairs in response to read column selection signals during a read operation;

a write column decoder for generating the write column selection signals to select a predetermined number of write column selection gates among the plurality of write column selection gates by inputting a column address during the write operation;

a read column decoder for generating the read column selection signals to select a predetermined number of read column selection gates among the plurality of read column selection gates by inputting the column address during the read operation;

a predetermined number of global write line pairs connected to a predetermined number of local write line pairs of each of the plurality of memory cell array blocks;

a predetermined number of global read line pairs connected to a predetermined number of local read line pairs of each of the plurality of memory cell array blocks;

a data input circuit between the at least one data input pad and the predetermined number of global write line pairs for transmitting data input from the at least one data input pad ~~a predetermined number of data input pads~~ to the predetermined number of global write line pairs;

a data output circuit between the at least one data output pad and the global read line pairs for outputting data transmitted from the predetermined number of global read line pairs to the at least one data output pad ~~a predetermined number of data output pads~~; and

a command decoder for decoding externally input command signals and generating a write command for the write operation and a read instruction for the read operation, wherein the command decoder decodes the command signals and further generates the write and the read commands for performing the write and the read operations simultaneously, and wherein the data transmitted from the at least one data input pad is transmitted during the write operation and the data output to the at least one data output pad is output during the read operation simultaneously.

9. (Canceled)

10. (Original) The semiconductor memory device according to claim 8, further

comprising:

a first switch for transmitting data input to a predetermined number of data input pads to the data input circuit in response to a control signal, and transmitting data transmitted from the data output circuit to a predetermined number of data output pads; and

a second switch for transmitting data input through the predetermined number of data output pads to the data input circuit in response to an inverted signal of the control signal, and transmitting data output from the data output circuit to the predetermined number of data input pads.

11. (Previously Presented) A method for writing and reading data to and from a semiconductor memory device comprising the steps of:

transmitting data input through a first pad to a write line pair during a write operation, and data output from a memory cell array to a read line pair during a read operation; and

transmitting data transmitted to the write line pair to the memory cell array during a write operation, and outputting data transmitted to the read line pair through a second pad during a read operation, wherein the write operation and the read operation are performed simultaneously.

12. (Original) The method according to claim 11, wherein the write operation and the read operation are performed independently.

13. (Canceled)

14. (Currently Amended) A method for writing and reading data to and from a semiconductor memory device comprising the steps of:

transmitting data input through a data input ~~(output)~~ pad on an input side of a data input circuit to a global write line pair on an output side of the data input circuit during a write operation, and transmitting data stored in a memory cell array to a local read line pair during a read operation in response to a read column selection signal;

transmitting data transmitted to the global write line pair to a local write line pair in

response to a write column selection signal during the write operation, and transmitting data transmitted to the local read line pair to a global read line pair during the read operation; and

transmitting data transmitted to the local write line pair to the memory cell array during the write operation, and transmitting data transmitted to the global read line pair on an input side of a data output circuit to ~~through~~ a data output ~~(input)~~ pad on an output side of the data output circuit during the read operation, wherein the data transmitted through the data input pad and the data transmitted through the data output pad ~~write operation and the read operation~~ are ~~performed~~ transmitted simultaneously.

15. (Original) The method according to claim 14, wherein the write operation and the read operation are performed independently.

16. (Canceled)

17. (Currently Amended) A semiconductor memory device comprising:

a memory cell array including a plurality of memory cell array blocks each including a plurality of memory cells connected between a plurality of word lines and a plurality of bit line pairs;

a predetermined number of local write line pairs of each of the plurality of memory cell array blocks for inputting data in each of the plurality of memory cell array blocks;

a predetermined number of local read line pairs of each of the plurality of memory cell array blocks for outputting data of each of the plurality of memory cell array blocks;

a plurality of write column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local write line pairs in response to a write column selection signal during a write operation;

read column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local read line pairs in response to a read column selection signal during a read operation;

a predetermined number of global write line pairs connected to the predetermined number

of local write line pairs of each of the plurality of memory cell array blocks, wherein the predetermined number of global write line pairs receives data input from at least one data input pad; and

a predetermined number of global read line pairs connected to the predetermined number of local read line pairs of each of the plurality of memory cell array blocks, wherein the predetermined number of global read line pairs outputs data transmitted from the predetermined number of global read line pairs to at least one data output pad, and wherein the data transmitted from the predetermined number of global read line pairs is received by the at least one data output pad and the data input from at least one data input pad is input through the at least one data input pad simultaneously; and

a command decoder for decoding externally input command signals and generating a write command for the write operation and a read command for the read operation, wherein the command decoder further generates write and read commands for performing the write and the read operations simultaneously after decoding the commands.

18. (Previously Presented) The semiconductor memory device according to claim 17, further comprising:

a first switch for transmitting data input through a predetermined number of data input pads to the predetermined number of global line pairs in response to a control signal, and outputting data transmitted from the predetermined number of global read line pairs to a predetermined number of data output pads; and

a second switch for transmitting data input through the predetermined number of data output pads to the predetermined number of global line pairs in response to an inverted signal of the control signal, and outputting data transmitted from the predetermined number of global read line pairs to the predetermined number of data input pads.

19. (Previously Presented) A semiconductor memory device comprising:

a memory cell array including a plurality of memory cell array blocks each including a plurality of memory cells connected between a plurality of word lines and a plurality of bit line

pairs;

a predetermined number of local write line pairs of each of the plurality of memory cell array blocks for inputting data in each of the plurality of memory cell array blocks;

a predetermined number of local read line pairs of each of the plurality of memory cell array blocks for outputting data of each of the plurality of memory cell array blocks;

a plurality of write column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local write line pairs during a write operation;

read column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local read line pairs during a read operation;

a write column decoder for generating write column selection signals to select a predetermined number of write column selection gates among the plurality of write column selection gates by inputting a column address during the write operation;

a read column decoder for generating read column selection signals to select a predetermined number of read column selection gates among the plurality of read column selection gates by inputting the column address during the read operation;

a predetermined number of global write line pairs connected to a predetermined number of local write line pairs of each of the plurality of memory cell array blocks;

a predetermined number of global read line pairs connected to a predetermined number of local read line pairs of each of the plurality of memory cell array blocks;

a data input circuit for transmitting data input to a predetermined number of data input pads to the predetermined number of global write line pairs;

a data output circuit for outputting data transmitted from the predetermined number of global read line pairs to a predetermined number of data output pads; and

a command decoder for decoding externally input command signals and generating a write command for the write operation and a read instruction for the read operation;

a first switch for transmitting data input to a predetermined number of data input pads to the data input circuit in response to a control signal, and transmitting data transmitted from the

data output circuit to a predetermined number of data output pads; and

a second switch for transmitting data input through the predetermined number of data output pads to the data input circuit in response to an inverted signal of the control signal, and transmitting data output from the data output circuit to the predetermined number of data input pads.

20. (Previously Presented) The semiconductor memory device according to claim 19, wherein the command decoder decodes the command signals and further generates the write and the read commands for performing the write and the read operations simultaneously.

21. (New) A semiconductor memory device comprising:

a memory cell array including a plurality of memory cell array blocks each including a plurality of memory cells connected between a plurality of word lines and a plurality of bit line pairs;

a predetermined number of local write line pairs of each of the plurality of memory cell array blocks for inputting data in each of the plurality of memory cell array blocks;

a predetermined number of local read line pairs of each of the plurality of memory cell array blocks for outputting data of each of the plurality of memory cell array blocks;

a plurality of write column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local write line pairs during a write operation;

read column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local read line pairs during a read operation;

a write column decoder for generating write column selection signals to select a predetermined number of write column selection gates among the plurality of write column selection gates by inputting a column address during the write operation;

a read column decoder for generating read column selection signals to select a

predetermined number of read column selection gates among the plurality of read column selection gates by inputting the column address during the read operation;

a predetermined number of global write line pairs connected to a predetermined number of local write line pairs of each of the plurality of memory cell array blocks;

a predetermined number of global read line pairs connected to a predetermined number of local read line pairs of each of the plurality of memory cell array blocks;

a data input circuit for transmitting data input from a predetermined number of data input pads to the predetermined number of global write line pairs;

a data output circuit for outputting data transmitted from the predetermined number of global read line pairs to a predetermined number of data output pads;

a command decoder for decoding externally input command signals and generating a write command for the write operation and a read instruction for the read operation, wherein the command decoder decodes the command signals and further generates the write and the read commands for performing the write and the read operations simultaneously;

a first switch for transmitting data input to the predetermined number of data input pads to the data input circuit in response to a control signal, and transmitting data transmitted from the data output circuit to the predetermined number of data output pads; and

a second switch for transmitting data input through the predetermined number of data output pads to the data input circuit in response to an inverted signal of the control signal, and transmitting data output from the data output circuit to the predetermined number of data input pads.

22. (New) A semiconductor memory device comprising:

a memory cell array including a plurality of memory cell array blocks each including a plurality of memory cells connected between a plurality of word lines and a plurality of bit line pairs;

a predetermined number of local write line pairs of each of the plurality of memory cell array blocks for inputting data in each of the plurality of memory cell array blocks;

a predetermined number of local read line pairs of each of the plurality of memory cell

array blocks for outputting data of each of the plurality of memory cell array blocks;

a plurality of write column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local write line pairs during a write operation;

read column selection gates of each of the plurality of memory cell array blocks for transmitting data between the plurality of bit line pairs and the predetermined number of local read line pairs during a read operation;

a predetermined number of global write line pairs connected to the predetermined number of local write line pairs of each of the plurality of memory cell array blocks;

a predetermined number of global read line pairs connected to the predetermined number of local read line pairs of each of the plurality of memory cell array blocks;

a command decoder for decoding externally input command signals and generating a write command for the write operation and a read command for the read operation, wherein the command decoder further generates write and read commands for performing the write and the read operations simultaneously after decoding the commands;

a first switch for transmitting data input through a predetermined number of data input pads to the predetermined number of global line pairs in response to a control signal, and outputting data transmitted from the predetermined number of global read line pairs to a predetermined number of data output pads; and

a second switch for transmitting data input through the predetermined number of data output pads to the predetermined number of global line pairs in response to an inverted signal of the control signal, and outputting data transmitted from the predetermined number of global read line pairs to the predetermined number of data input pads.